DIO4264
PC-104 Digital I/O Card

User's Manual (V1.0)

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Correction record

Version	Record

Contents

Notes on hardware installation

Please follow step by step as you are installing the control cards.

1. Be sure your system is power off.
2. Be sure your external power supply for the wiring board is power off.
3. Plug your control card in slot, and make sure the golden fingers are put in right contacts.
4. Fasten the screw to fix the card.
5. Connect the cable between the card and wiring board.
6. Connect the external power supply for the wiring board.
7. Recheck everything is OK before system power on.
8. External power on.

Congratulation! You have it.

For more detail of step by step installation guide, please refer the file “installation.pdf “ on the CD come with the product or register as a member of our user’s club at:

http://automation.com.tw/

to download the complementary documents.

1. Forward

Thank you for your selection of JAC's product DIO4264 DIGITAL I/O card for PC104 compatible industrial PC.

This card is a FPGA based design that gives the maximum flexibility of implementation. It has 48 point 82C55 mode 0 compatible I/O with extend driving capacity (adopt 74HC245 as buffer). Not only the emulation of 82C55 functions, we also provide 16 extra nibble programmable I/O for your best performance/cost result.

For the most convenience of the user the connectors are OPTO22 compatible and the circuit diagram of the card also provided.

Other DIO series products:

DIO9201	16 channel input and 16 channel output isolated digital I/O card (ISA bus)
DIO2232	32 channel input and 32 channel output isolated digital I/O card (ISA bus)
DIO2248	48 channel input and 16 channel output isolated digital I/O card (ISA bus)
DIO2264	64 channel input isolated digital I/O card (ISA bus)
DIO3206	48 channel TTL digital I/O Card (PCI bus)
DIO3208B	8 channel input and 8 channel relay output isolated digital I/O card (PCI bus)
DIO3216B	16 channel input and 16 channel output isolated digital I/O card (PCI bus)
DIO3217	16 channel input and 16 channel output isolated digital I/O card (PCI bus) with multifunction timer/counter
DIO3232	32 channel input and 32 channel output isolated digital I/O card (PCI bus)
DIO3248	48 channel input and 16 channel output isolated digital I/O card (PCI bus)
DIO3264	64 channel input isolated digital I/O card (PCI bus)
DIO6208	8 channel input and 8 channel relay output isolated digital I/O PCI-104 Module
DIO6216	16 channel input and 16 channel relay output isolated digital I/O PCI-104 Module

Any comment is welcome,
please visit our website
http://www.automation.com.tw/
http://www.automation-js.com/ for the up to date information.

2. Packing list

2.1	DIO4264 PC-104 digital I/O card	x 1
2.2	Manual Cd rom	x 1
2.3	Accessories	x 1

3. Features

3.1 48 digital I/O lines emulate Two 82C55A PPIs

3.2 16 extra nibble programmable digital I/O

3.3 Dual 50-pin connectors for OPTO22 compatible module racks

3.4 FPGA based design

3.5 Wide power range: 3.6-6.0Vdc

3.6 EXT/INT irq trigger, programmable irq no.

3.7 Circuit diagram provided for potential customer to field change

4. Specifications

Power Requirement

4.1.1 Power supply range: 3.6 – 5.5Vdc

4.1.2 Power consumption: 150mA @5V

Input Stage (@Vcc=4.5V)

4.1.3 Logic high voltage: 3.15V(min)

4.1.4 Logic low voltage: 1.35(max)

4.1.5 Input high current: 1uA(max)

4.1.6 Input low current: -1uA(max)

Output Stage (@Vcc=4.5V)

4.1.7 Logic high voltage: 3.84V(min) @6mA load

4.1.8 Logic low voltage: 0.33V(min) @6mA load

4.1.9 Output high current: -35mA(max)

4.1.10 Output low current: 35mA(max)

Interrupt

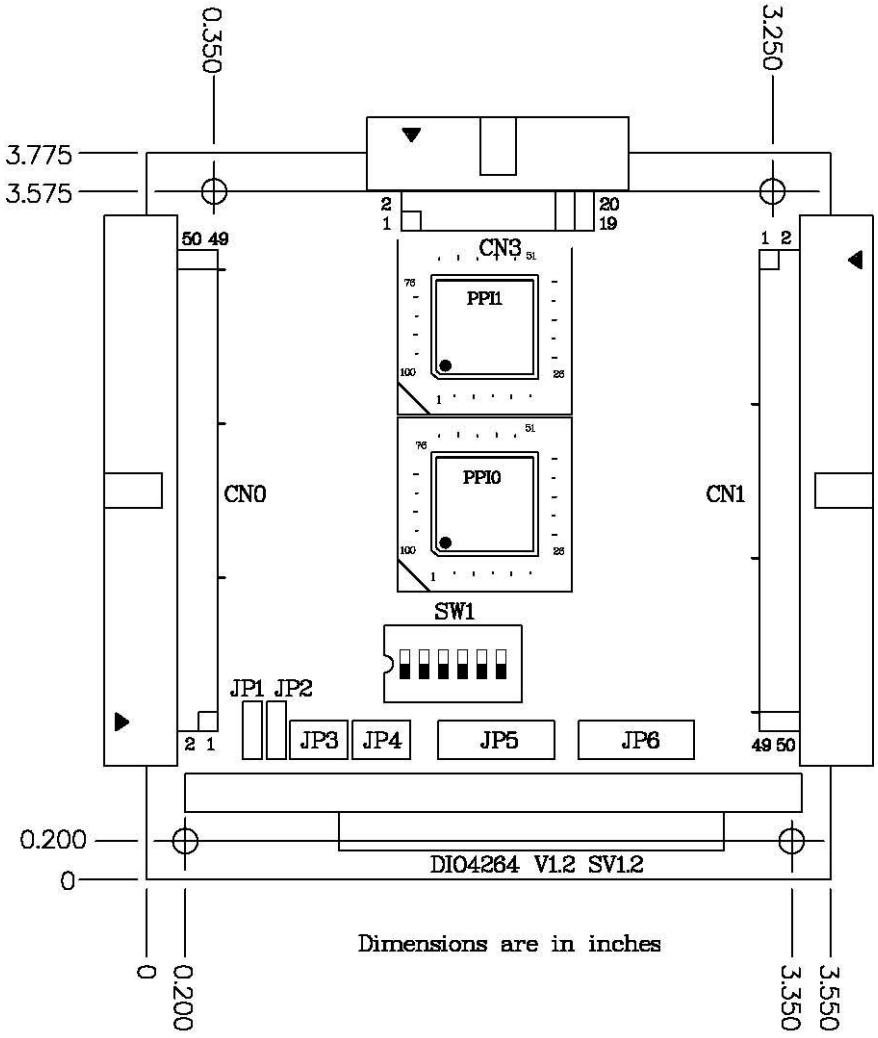
4.1.11 Mode: INTernal/EXTernal

4.1.12 Enable/Disable: PC04/PC14

4.1.13 Trigger in: PC00/PC10

4.1.14 Irq no.:irq2-irq7,jumper selectable

5. Layout and dimensions



6. Pin definitions

6.1 PPI connectors

PPI0 I/O connector

CN0

PC07	1	2	GND
PC06	3	4	GND
PC05	5	6	GND
PC04	7	8	GND
PC03	9	10	GND
PC02	11	12	GND
PC01	13	14	GND
PC00	15	16	GND
PB07	17	18	GND
PB06	19	20	GND
PB05	21	22	GND
PB04	23	24	GND
PB03	25	26	GND
PB02	27	28	GND
PB01	29	30	GND
PB00	31	32	GND
PA07	33	34	GND
PA06	35	36	GND
PA05	37	38	GND
PA04	39	40	GND
PA03	41	42	GND
PA02	43	44	GND
PA01	45	46	GND
PA00	47	48	GND
+5Vout	49	50	GND

PPI1 I/O connector

CN1

PC17	1	2	GND
PC16	3	4	GND
PC15	5	6	GND
PC14	7	8	GND
PC13	9	10	GND
PC12	11	12	GND
PC11	13	14	GND
PC10	15	16	GND
PB17	17	18	GND
PB16	19	20	GND
PB15	21	22	GND
PB14	23	24	GND
PB13	25	26	GND
PB12	27	28	GND
PB11	29	30	GND
PB10	31	32	GND
PA17	33	34	GND
PA16	35	36	GND
PA15	37	38	GND
PA14	39	40	GND
PA13	41	42	GND
PA12	43	44	GND
PA11	45	46	GND
PA10	47	48	GND
+5Vout	49	50	GND

6.2 Extra 16 points nibble programmable I/O connector

CN3

PD00	1	2	PD01
PD02	3	4	PD03
PD04	5	6	PD05
PD06	7	8	PD07
PD10	9	10	PD11
PD12	11	12	PD13
PD14	13	14	PD15
PD16	15	16	PD17
GND	17	18	GND
+5Vout	19	20	+5Vout

7. Installations

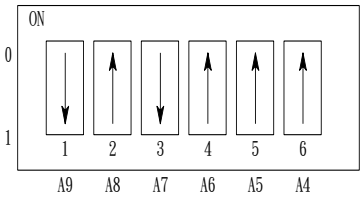
7.1 Base address setting

The modules occupies 12 contiguous I/O address and configured in 16 address per block by the DIP switch.

For example, to set I/O address at 280H:

DIP1	DIP2	DIP3	DIP4	DIP5	DIP6
A9	A8	A7	A6	A5	A4
1	0	1	0	0	0

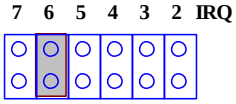
DIP SW SETTING：(280H)



7.2 Interrupt setting

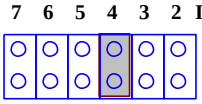
The interrupt can be set separately for PPI0 and PPI1 from irq2 to irq7 as you need.

PPI0 irq jumpers



JP5

PPI1 irq jumpers

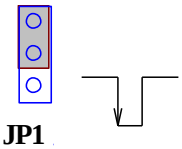


JP6

7.3 Irq trigger level setting

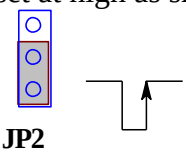
The input level of PC00 (PPI0 port C bit 0) to trigger irq can be set by JP1, and PC10 (PPI1 port C bit 0) by JP2. Set to low means a transition of PC00 /PC10 from high to low transition triggers irq, and high means low to high transition triggers irq.

PPI0 trigger level
(set at low as shown)



JP1

PPI1 trigger level
(set at high as shown)



JP2

7.4 Irq mode

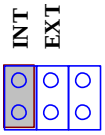
The are 3 irq mode can be set separately for PPI0 and PPI1.

DIS: disable interrupt

EXT: external trigger, the input of PC00/PC10 can GENERATE interrupt by the LOW state of PC04/PC14, and DISABLED by theHIGH state of PC04/PC14.

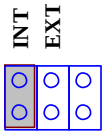
INT: internal register controlled, the input the input of PC00/PC10 can GENERATE interrupt by SET the bit0 of IrqnMode register to 1, and DISABLED by set it to 0 . The Irq should be cleared at the end of interrupt service routine by READ IrqnMode Register.

PPI0 irq mode
(set at disable as shown)



JP3

PPI1 irq mode
(set at disable as shown)



JP4

8. Configurations

8.1 I/O port function

Note: All the ports are pulled high by 10K resistors, during power on take care of the possible logic high output.

Port Address	Mnemonic	Read	Write
Base+0	PPI0A	Input data of 8255-0 port A	Output data to 8255-0 port A
Base+1	PPI0B	Input data of 8255-0 port B	Output data to 8255-0 port B
Base+2	PPI0C	Input data of 8255-0 port C	Output data to 8255-0 port C
Base+3	PPI0Mode	N/A	8255-0 Mode register
Base+4	PPI1A	Input data of 8255-1 port A	Output data to 8255-1 port A
Base+5	PPI1B	Input data of 8255-1 port B	Output data to 8255-1 port B
Base+6	PPI1C	Input data of 8255-1 port C	Output data to 8255-1 port C
Base+7	PPI1Mode	N/A	8255-1 Mode register
Base+8	PORT0D	Input data of Port 0D	Output data to Port 0D
Base+9	PORT1D	Input data of Port 1D	Output data to Port 1D
Base+A	Irq0Mode	Clear Irq of PPI0	Set/reset Irq of PPI0 in INT mode
Base+B	Irq1Mode	Clear Irq of PPI1	Set/reset Irq of PPI1 in INT mode

8.2 Mode register

PPInMode (8255-n Mode Register)								
b7	b6	b5	b4	b3	b2	b1	b0	R/W
1	0	0	PAn	PCn4-n7 PDn4-n7	0	PBn	PCn0-n3 PDn0-n3	Write only

n: the PPI number, maybe 0 or 1

PAn: 1=portA as input

0=portA as output

PCn4-n7 / PDn4-n7: 1=portC / portD high nibble as input

0=portC / portD high nibble as output

PBn: 1=portB as input

0=portB as output

PCn0-n3 / PDn0-n3: 1=portC / portD low nibble as input

0=portC / portD low nibble as output

Note: PortD is the extra port and its attribute as input or output is depend on the attribute of portC.

8.3 Irq mode register

IrqnMode (Irqn Mode Register)								
b7	b6	b5	b4	b3	b2	b1	b0	R/W
0	0	0	0	0	0	0	DIS/ENA	Read/ Write

DIS/ENA: 1= enable INT mode irq

0= disable INT mode irq

Note: 1. Read will return a null data, but clears the latched irq.

2. The IrqnMode register only effect at the jumper (JP3/JP4) set at INT mode.

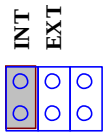
9. Programming

9.1 Simple I/O

Here is the application for a simple control, which needs PortA as byte output, PortC and PortD low nibble as output else as input. This application needs no interrupt.

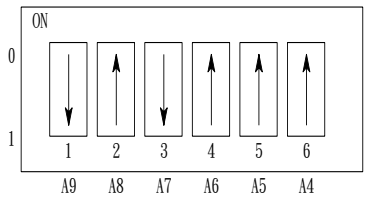
The conditions as follows:

- No interrupt
- Base address set at 0x280
- Port0A as byte output
- Port0B as byte input
- Port0C_l as nibble output
- Port0C_h as nibble input
- Port0D_l as nibble output
- Port0D_h as nibble input



JP3

Disable IRQ



Address DIP switch setting

Example coding with Basic language

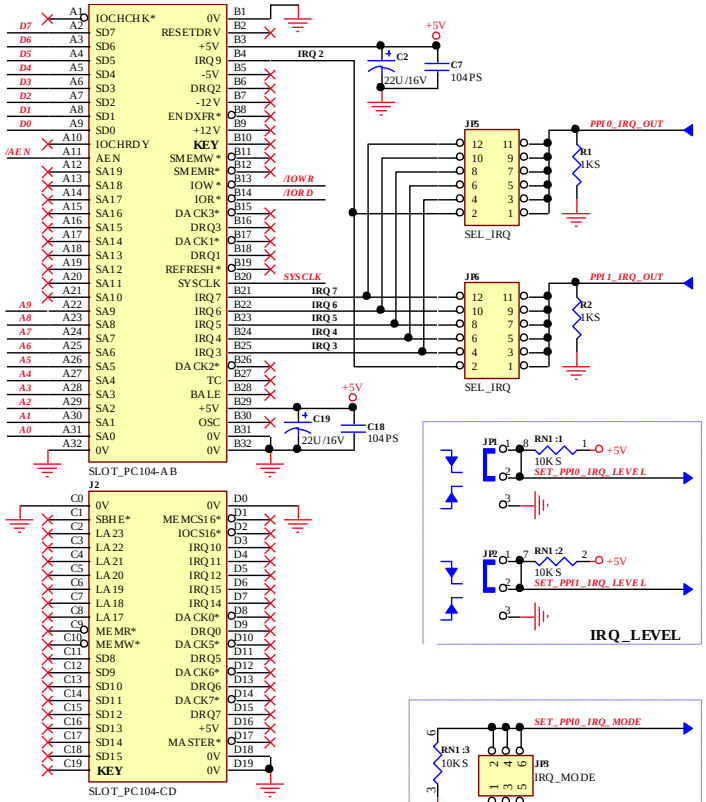
```
10   CLS
20   PORT%=&H280                    'REM Base address
30   OUT PORT%+3,&H83     'REM program PPI0M; P0A,P0C_l,P0D_l: output;
'REM P0B,P0C_h,P0D_h: input
40   FOR I=0 TO 255
50   OUT PORT%+0,I                  'REM write data to P0A
OUT PORT%+2,I                  'REM write data to P0C_l
70   OUT PORT%+8,I                  'REM write data to P0D_l
80   B=INP(PORT%+1)                 'REM read data from P0B
90   C=INP(PORT%+2)                 'REM read data from P0C_h
100   D=INP(PORT%+8)            'REM read data from P0D_h
110   PRINT B,C,D,I                 'REM check data
NEXT I
130   END
```

Example coding with C language

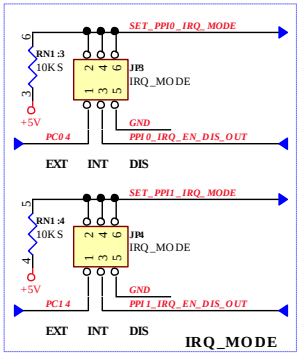
```
#include <stdio.h>
#include <conio.h>
#include <process.h>
#include <dos.h>

Main ( )
{
  int base= 0x280;              /* set base i/o address at 0x280 */
  int B,C,D;
  outportb (base+3,0x83);       /* program PPI0M; P0A,P0C_l,P0D_l: output;
                                                    P0B,P0C_h,P0D_h: input */
  for (i=0;i<=255;i++)
  {
      outportb (base+0,i) ; /* write data to P0A */
      outportb (base+2,i) ; /* write data to P0C_l */
      outportb (base+8,i) ; /* write data to P0D_l */
      B=inportb(base+1) ; /* read from P0B */
      C=inportb(base+2) ; /* read from P0C_h */
      D=inportb(base+8) ; /* read from P0D_h */
      printf ("B=%x,C=%x,D=%x\n",B,C,D);
}
```

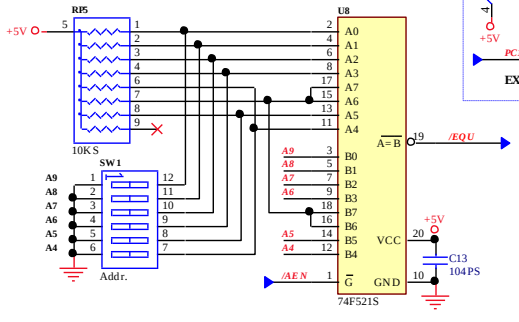
10. Circuit diagram

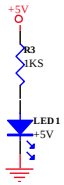


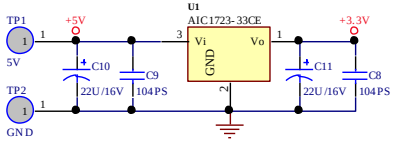
JP1(JP2) IRQ_LEVEL
1-2 short => Lo Level
2-3 short => Hi Level

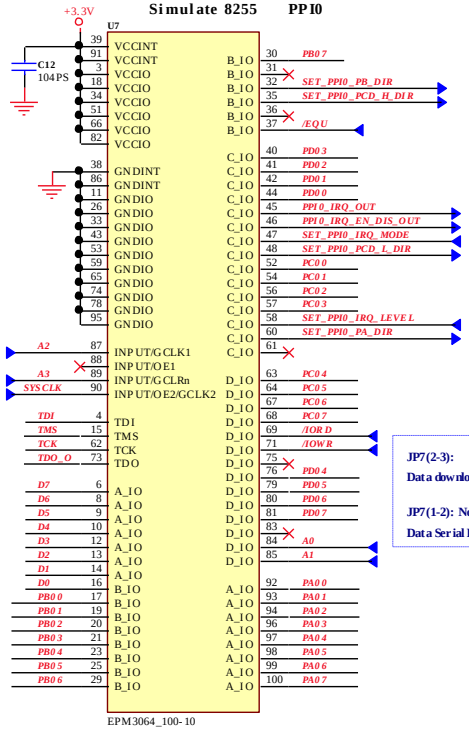


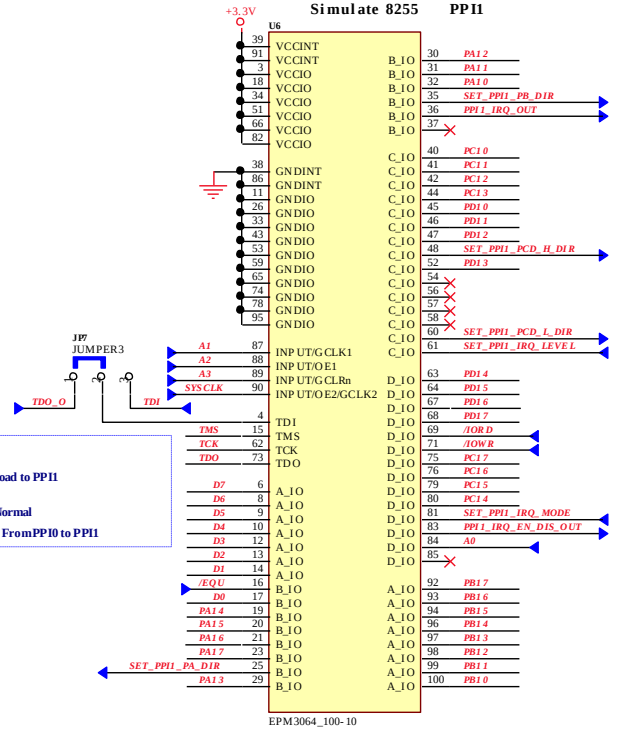
IRQ source from PC00(pc10)
JP3(JP4)
1-2 short => IRQ by PC04(pc14) EN/DIS
3-4 short=> IRQ by SOFT EN/DIS
5-6 short => IRQ always DIS
OPEN => IRQ always ENA
IRQ_MODE











JP7(2-3):
Data download to PPI1

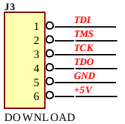
JP7(1-2): Normal
Data Serial From PPI0 to PPI1

base+0 ==> Read/Write PPI0_port A
base+1 ==> Read/Write PPI0_port B
base+2 ==> Read/Write PPI0_port C
base+3 ==> Set PPI0 PortA,B,C,D I/O Mode

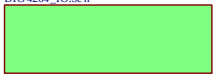
base+4 ==> Read/Write PPI1_port A
base+5 ==> Read/Write PPI1_port B
base+6 ==> Read/Write PPI1_port C
base+7 ==> Set PPI1 PortA,B,C,D I/O Mode

base+8 ==> Read/Write PPI0_port D
base+9 ==> Read/Write PPI1_port D

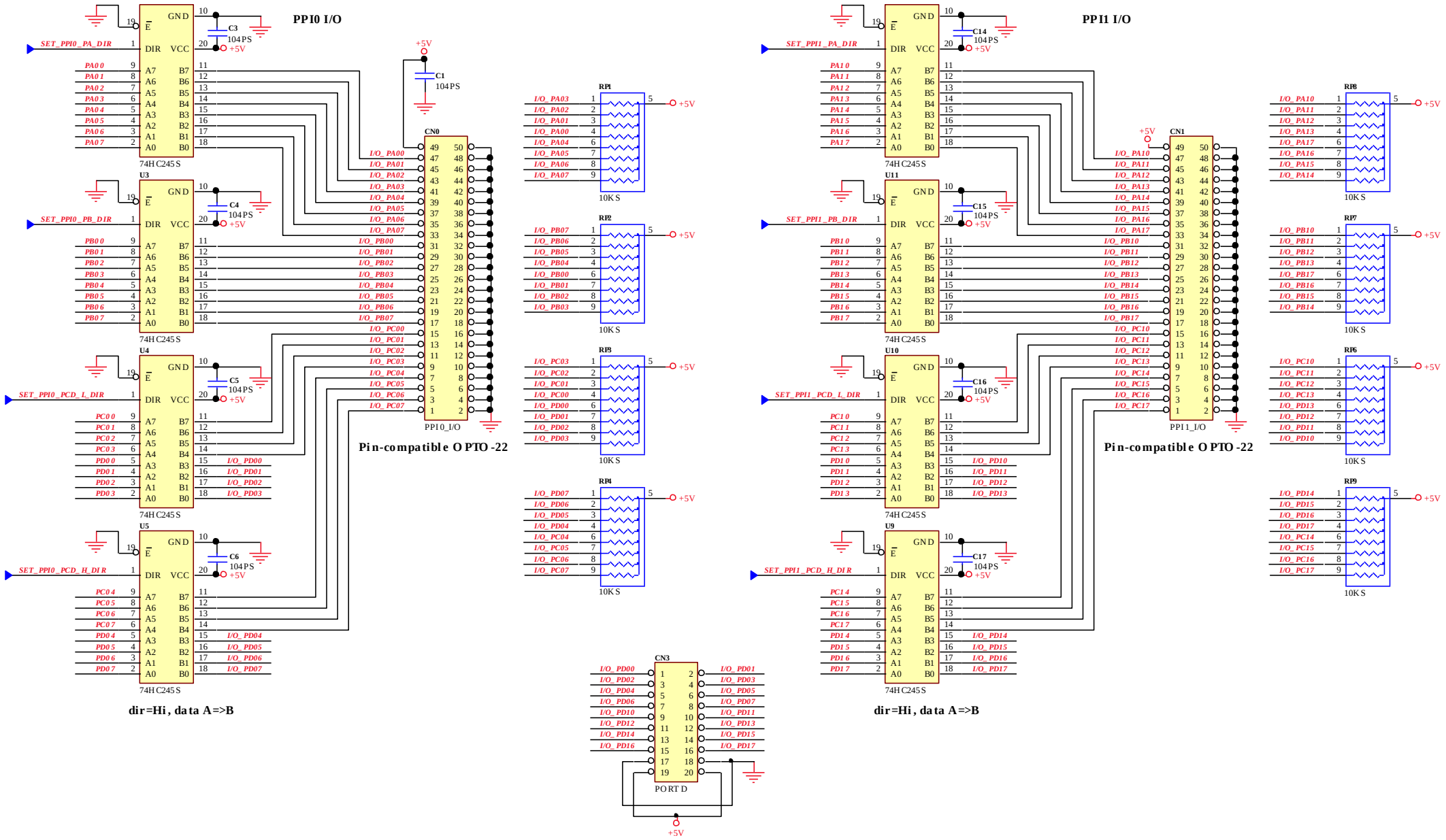
base+A ==> Write : Ena/Dis PPI0_IRQ(Data bit0=1 Ena;Data bit0=0 Dis),Read : Clr PPI0_IRQ
base+B ==> Write : Ena/Dis PPI1_IRQ(Data bit0=1 Ena;Data bit0=0 Dis),Read : Clr PPI1_IRQ



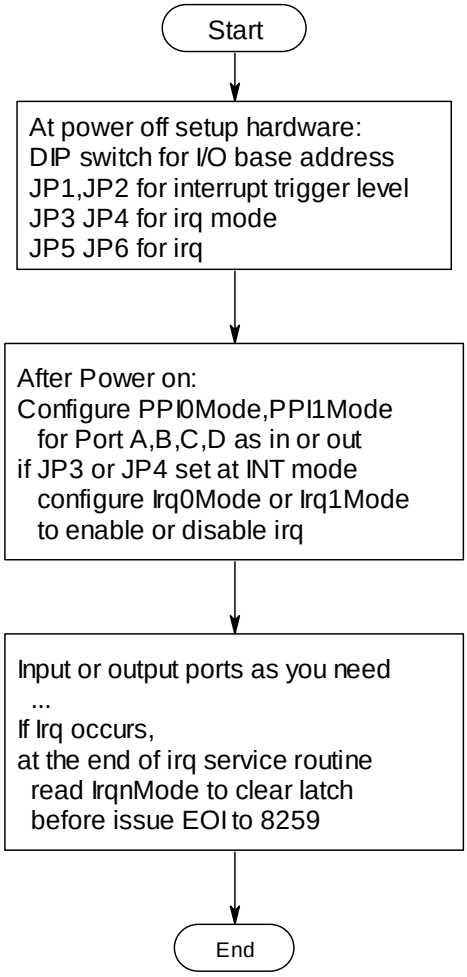
DIO4264_IO
DIO4264_IO.Sch



Programmable-Peripheral-Interface


PPI0 I/O
PPI1 I/O
74HC245S
PPI0_I/O
PPI1_I/O
Pin-compatible OPTO-22
dir=Hi, data A=>B
10KS
104PS
+5V
PORTD

11. Flow for initial application



12. Ordering information

PRODUCT	DESCRIPTIONS
DIO4264	PC-104 64 I/O card (Emulate 2 8255 with higher Output capacity)
M23220	1.5M long ,50pin flat cable
M23207	20 pin flat cable 1.5M
M23209	20 pin flat cable 3.0M